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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,123	06/29/2001	Katsumi Kikuchi	Q65269	5729

7590 02/18/2004

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,123	KIKUCHI ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 42-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,15-17 and 42-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/12/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 1, 2003 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 2, 3, 5, 6, 7, 15, 16, 17, 42, 43, 44 and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by Ho, U.S. Patent 6,287,890 B1.

5. Pertaining to claim 1, Ho discloses a semiconductor device as claimed. See **FIG. 1**, where Ho teaches a semiconductor package board comprising:

a metal base plate **14** having an opening suited for receiving

therein a semiconductor chip **16**; and

a multilayer wiring film **12** formed on said metal base plate;

said multilayer wiring film having a first surface, said first surface having a first region in contact with said metal base plate, said first surface having a second region exposed by said opening in said metal base plate; and

a plurality of first metal pads formed in said second region.

6. Pertaining to claim 2, Ho teaches the semiconductor package board according to claim 1, wherein said multilayer wiring film includes a plurality of wiring layers and a plurality of insulating layers alternately stacked upon one another, via holes formed in said plurality of insulating layers for interconnecting, said plurality of wiring layers, and a plurality of second metal pads formed on a second surface of said multilayer wiring film opposite to said first surface, and wherein said second metal pads are electrically connected to said first metal pads through said wiring layers and said via holes.

7. Pertaining to claim 3, Ho teaches the semiconductor package board according to claim 1, wherein said multilayer wiring film has a metallic film in contact with a periphery of said opening of said metal base plate.

8. Pertaining to claim 5, Ho fails to teach the semiconductor package board according to claim 1, wherein said metal base plate comprises at least one metal selected from the group consisting of stainless steel, iron, nickel, copper, and aluminum, or an alloy thereof (column 6, lines 54-60).

9. Pertaining to claim 6, Ho teaches the semiconductor package board according, to claim 1, wherein said first metal Pads are covered by a surface layer comprising at least one metal selected from the group consisting of gold, tin, and solder, or an alloy thereof (column 7, lines 35-46).

10. Pertaining to claim 7, Ho teaches the semiconductor package board according to claim 2, wherein each of said insulating layers comprises one or more of organic resins selected from the group consisting of an epoxy resin, an epoxy acrylate resin, an urethan acrylate resin, a polyester resin, a phenol resin, a polyimide resin, a benzocyclobutene (BCB), and a polybenzoxazole (PBO).

11. Pertaining to claim 15, Ho teaches a semiconductor device comprising the semiconductor package board according to claim 1, and a semiconductor chip disposed within said opening and connected to said first metal pads.

12. Pertaining to claim 16, Ho teaches the semiconductor device according to claim 15, wherein said semiconductor chip is flip-chip bonded to said first metal pads by a

material made of either a metal having a low melting point or a conductive resin.

13. Pertaining to claim 17, Ho teaches the semiconductor device according to claim 15, wherein said semiconductor chip is connected to said multilayer wiring film by at least one material selected from the group consisting of a metal having a low melting point, an organic resin, and a resin containing a metal.

14. Pertaining to claim 42, Ho teaches the semiconductor package board according to claim 1, wherein said first metal pads comprise a surface, a portion of said surface is not in direct contact with said multilayer wiring film, said portion being coplanar with said multilayer wiring film.

15. Pertaining to claim 43, Ho teaches the semiconductor package board according to claim 1, wherein said first metal pads comprise a surface, a portion of said surface is not indirect contact with said multilayer wiring film, said portion being recessed toward said first surface of said multilayer wiring film.

16. Pertaining to claim 44, Ho teaches the semiconductor package board according to claim 1, wherein the surface of said first metal pads is recessed from the surface of said multilayer wiring film.

17. Pertaining to claim 45, Ho teaches a semiconductor package board comprising:

a base plate having an opening; and

a multilayer wiring film formed on said metal base plate, said multilayer wiring film having a first surface in contact with said base plate and mounting thereon a plurality of first metal pads (line 9 of Ho) within a region exposed from said opening of said metal base plate, wherein surface of the first metal pads is recessed from the surface of the multilayer wiring film.

Objections

18. Claims 4, 8, 9, 10, 11, 12, 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on 9:00 AM-5:00 PM.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached at 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC